Leading Semiconductor Design Revolution with SiFive/RISC-V Core IP Enabling Embedded Intelligence
We invented RISC-V

SiFive’s founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercial implementation of the RISC-V Instruction Set Architecture (ISA) since 2010.

Andrew Waterman
Chief Engineer

Yunsup Lee
CTO

Krste Asanovic
Chief Architect

“SiFive Recognized as Most Respected Private Semiconductor Company”
About SiFive

Worldwide Presence
13 Offices
350+ Employees (275+ Engineers)
300+ Tapeouts

World-class expertise
- Inventors of RISC-V
- Chip Design in the Cloud
- RTL Design & Verification
- FPGA & Emulation
- Physical Design
- Wafer Fabrication
- Board Design
- Full Silicon Validation
SiFive社日本国内代理店 DTSインサイトが目指すビジネス領域

ハードウェア/ファームウェア組込などの得意領域を活かし、お客様のあらゆるニーズにお応えするOne Stop Solutionをご提案いたします

New Business
LSIデザインサービス
・LSIデザインサービス
・株式会社SSC様と協業
・RISC-V開発ボード環境
・RISC-Vデバッガ
・FW移行サービス

プロセッサIP（RISC-V）を題材にスタート

Mainstream
組込みSW開発

・組込みソフトウェア開発
・ハードウェア開発
  •（回路設計、PCB設計、機構・筐体設計から試作製造、量産）
  •デバッガ(ICEなど)
  •データモニターツール
  •動的テスト/解析ツール
  •ソフトウェア構造分析ツール
  •トレーサビリティ管理ツール
What we do

Leaders in RISC-V

- Inventors of RISC-V
- Most complete product line of CPU IP: from microcontrollers, to embedded, to high-performance multi-core processors
- Very easy to customize

Leaders in taking Semiconductors to the Cloud

- Leverages software, high-level design, and automation
- Dramatically reduce cost and increase innovation
- Builds custom CPU IP and ASICs

Leaders in traditional ASICs (CSoC BU)

- Flexible engagement model (Spec2Chip, RTL, Netlist, GDS2, Production)
- Robust design methodology and extensive experience in integration of IP
- Manufacturing excellence
- Full responsibility of production supply chain
Introducing a fundamentally new approach to developing processor IP and custom SoCs (CSoCs)
Custom SoC BU: Full Turnkey Custom SoC Solution Capability

Product Requirement & Specification

Architecture Analysis, RTL Design & Verification

IP Development, Selection & Integration

Software Design, Development & Test

FPGA & Emulation

Physical Design

Post Silicon Validation & Software Bring-up

Board Design

Test & Production Engineering

Package & Assembly

Wafer Fabrication
SiFive RISC-V Core IP Product Overview
SiFive Core IP: Efficient, High-Performance, Customizable Core IP

<table>
<thead>
<tr>
<th>SiFive RISC-V Core IP</th>
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</table>
| **E Cores**  
32-bit Embedded Cores  
- Edge Computing  
- Artificial Intelligence  
- Embedded IoT  
- Wearables | **S Cores**  
Industry leading 64-bit Embedded Cores  
- Embedded Intelligence  
- Storage/SSD  
- AR/VR  
- Machine Learning | **U Cores**  
High performance, 64-bit Application Processors  
- Linux applications  
- Datacenter Accelerators  
- Storage system controllers  
- Networking baseband |

- **Lowest Risk, Fastest Time to Market**  
  - SiFive IP is silicon-proven and our licensees are shipping  
  - Leaders in RISC-V standardization and new spec development  
  - Broadest portfolio of mature cores and a well-funded roadmap  
- **Unique features that scale across entire product portfolio**  
  - Single delivery with multiple cores, coherent memory subsystems, buses, assembled and verified by SiFive  
  - Highly Configurable, pre-integrated Verilog deliverables

- **Multiple Customization Options**  
  - Highly configurable cores to achieve application specific requirements  
  - Custom Instructions interface allows for differentiation enabled via the extensibility of the RISC-V ISA  
  - Subsystem, memory map, etc.. are all customizable

- **Faster, EfficientProcessors**  
  - Measured higher total performance and performance/mW vs similar designs in the same process node
NEW IP PARADIGM : SiFive Core Designer

• Annual subscription allows a customer’s engineers to access SiFive’s entire processor portfolio via a simple web interface
• Configuring SiFive’s processor IP is fast and easy
• A configured processor is generated in the cloud and the results are delivered to the user’s SiFive dashboard (RTL, SDK, test bench, docs)

SiFive CoreDesigner

Explore Before allows engineers to analyze their configured cores in their system simulations before committing to using them

• There is no processor modeling language to learn and no IP configuration tools to install
• FPGA bitstreams are provided to allow SW to run on a configured processor

RISC-V grants every user the right to modify their processor IP; SiFive has made it incredibly easy to do so.
BUSINESS MODEL

• Subscription-based license for SiFive Core Designer
  • Annual fee is based on which core series are included
  • SaaS model significantly reduces your IT and EDA support requirements
  • The most cost effective way of creating your own custom RISC-V cores
  • Allows for exploration of different configurations

• Predictable usage costs
  • Pricing is determined upfront and is valid during subscription term
  • Prepaid upfront and/or negotiated usage table for follow-on projects

Custom and Cost Effective

SiFive’s business model delivers all the benefits and saves you money
SiFive IP Portfolio

Choose your foundation

Core Series provide powerful capabilities for your product ideas. Choose one of our silicon-proven RISC-V Standard Cores—or customize a core to get the precise results that you need.

<table>
<thead>
<tr>
<th>Core Series</th>
<th>Area</th>
<th>Standard Cores</th>
<th>ARM Comparison</th>
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<tbody>
<tr>
<td>E2 Series</td>
<td></td>
<td>E20, E21, E24</td>
<td>M0, M0+, M3, M4, M23, M33</td>
</tr>
<tr>
<td>E3 Series</td>
<td></td>
<td>E31, E34</td>
<td>R4, R5</td>
</tr>
<tr>
<td>E7 Series</td>
<td></td>
<td>E76, E76-MC</td>
<td>M7, R7, R8</td>
</tr>
<tr>
<td>S5 Series</td>
<td></td>
<td>S51, S54</td>
<td>R4, R5</td>
</tr>
<tr>
<td>S7 Series</td>
<td></td>
<td>S76, S76-MC</td>
<td>M7, R7, R8</td>
</tr>
<tr>
<td>U5 Series</td>
<td></td>
<td>U54, U54-MC</td>
<td>A5, A7, A35, A53</td>
</tr>
<tr>
<td>U7 Series</td>
<td></td>
<td>U74, U74-MC</td>
<td>A55</td>
</tr>
</tbody>
</table>

Get best-in-class processor IP developed by the inventors of RISC-V and configure it to your exact specifications.
SiFive RISC-V Core IP Product Series

SiFive RISC-V Core IP

E Cores | S Cores
Industry leading 32-bit and 64-bit Embedded Cores

<table>
<thead>
<tr>
<th>7Series</th>
<th>3/5Series</th>
<th>2Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Performance Embedded</td>
<td>Small, Efficient, Performance</td>
<td>SiFive’s Most Efficient Series</td>
</tr>
<tr>
<td>Storage Networking Automotive</td>
<td>Industrial Modems Storage</td>
<td>Microcontrollers IoT Wearables</td>
</tr>
<tr>
<td>S76</td>
<td>S51</td>
<td>E21</td>
</tr>
<tr>
<td>S76-MC</td>
<td>S54</td>
<td>E24</td>
</tr>
<tr>
<td>E76</td>
<td>E31</td>
<td>E20</td>
</tr>
<tr>
<td>E76-MC</td>
<td>E34</td>
<td></td>
</tr>
</tbody>
</table>

U Cores
High performance 64-bit Application Cores

<table>
<thead>
<tr>
<th>7Series</th>
<th>5Series</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimized High-Performance</td>
<td>Multi-Core RISC-V Linux</td>
<td></td>
</tr>
<tr>
<td>SBC Networking Consumer</td>
<td>Low Cost Linux Industrial Gateways</td>
<td></td>
</tr>
<tr>
<td>U74</td>
<td>U54-MC</td>
<td></td>
</tr>
<tr>
<td>U74-MC</td>
<td>U54</td>
<td></td>
</tr>
</tbody>
</table>

Core Series are customizable to meet your requirements
Standard Cores are pre-configured, silicon-proven implementations
## Product Map

<table>
<thead>
<tr>
<th>E Cores</th>
<th>32-bit embedded cores</th>
<th>S Cores</th>
<th>64-bit embedded cores</th>
<th>U Cores</th>
<th>64-bit application cores</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>7 Series</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E7 Series</td>
<td>Compare to Cortex-M7 Quad-core 32-bit embedded processor</td>
<td>S7 Series</td>
<td>No 64-bit Cortex equivalent</td>
<td>U7 Series</td>
<td>Compare to Cortex-A55 MP4 Multicore: four U74 cores and one S76 core</td>
</tr>
<tr>
<td>E76-MC</td>
<td>Quad-core 32-bit embedded processor</td>
<td>S76-MC</td>
<td>Quad-core 64-bit embedded processor</td>
<td>U74-MC</td>
<td>Compare to Cortex-A55</td>
</tr>
<tr>
<td>E76</td>
<td>High performance 32-bit embedded core</td>
<td>S76</td>
<td>No 64-bit Cortex equivalent</td>
<td>U74</td>
<td>High performance Linux-capable processor</td>
</tr>
<tr>
<td><strong>3/5 Series</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E3 Series</td>
<td>Compare to Cortex-R5F E31 features + single-precision floating point</td>
<td>S5 Series</td>
<td>No 64-bit Cortex equivalent</td>
<td>U5 Series</td>
<td>Compare to Cortex-A53 Multicore application processor with four U54 cores and one S51 core</td>
</tr>
<tr>
<td>E34</td>
<td>Balanced performance and efficiency</td>
<td>S54</td>
<td>No 64-bit Cortex equivalent</td>
<td>U54-MC</td>
<td>Compare to Cortex-A53</td>
</tr>
<tr>
<td>E31</td>
<td></td>
<td>S51</td>
<td>Low-power 64-bit MCU core</td>
<td></td>
<td>Linux-capable application processor</td>
</tr>
<tr>
<td><strong>2 Series</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2 Series</td>
<td>Compare to Cortex-M4F E21 + single-precision floating point</td>
<td>S2 Series</td>
<td>No 64-bit Cortex equivalent</td>
<td>U5</td>
<td>Compare to Cortex-A53</td>
</tr>
<tr>
<td>E24</td>
<td></td>
<td>S21</td>
<td>Area-efficient 64-bit MCU core</td>
<td></td>
<td>Linux-capable application processor</td>
</tr>
<tr>
<td>E21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E21</td>
<td>User Mode, Atomics, Multiply, TIM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E20</td>
<td>Our smallest, most efficient core</td>
<td></td>
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</tr>
</tbody>
</table>
SiFive Core IP Already Covers 80% of ARM’s Cortex Roadmap

Additional Cores

- S77 • Vector Extensions
- E34/S34 • Floating Point
- S51 • 64-bit Option
- E27 • Vector Extensions
- E24 • Floating Point
SiFive 2/7 Series RISC-V Core IP
SiFive 2 Series RISC-V Core IP
SiFive Core IP
2 series:

SiFive’s **smallest** and most **efficient** RISC-V processor IP
E2 Series Features

The Smallest, Most Efficient RISC-V MCU Family

- **E2 Series core architectural overview**
  - RV32IMAFCV capable core
  - 2-3 stage, optional, Harvard Pipeline

- **RISC-V Vector extension support**
  - E27 Standard Core
  - Vector configurations available in SCD

- **Efficient memory accesses**
  - Ability to add multiple outbound Ports
  - Optional Tightly Integrated Memory (TIM)

- **First RISC-V core with support for the RISC-V Core Local Interrupt Controller (CLIC)**
  - Provides hardware interrupt prioritization and nesting

- **SiFive Custom Instruction Extension (SCIE)**
  - Easily add support for custom instructions
E20 Standard Core

• SiFive’s Most Efficient Standard Core
  – 0.023mm² in TSMC 28HPC for entire Core Complex including CLIC, Debug, and System Port
  – 1.1DMIPS/MHz, 2.4 Coremarks/MHz

• E20 Standard Core is optimized for Area and Power
  – Single Core Interface for all Instruction and Data accesses
  – 4 cycle hardware multiply
  – Single System Port Interface

• 4 Hardware breakpoint/watchpoints

• Extreme low latency interrupt handling
  • Execute first instruction of C handler in 6 cycles
  • Execute entire ISR in 18 cycles

Note: All area and power numbers do not include RAMs
*Core Complex includes the Core plus CLIC w/32 irq and 2 priority bits, Debug w/ 4 hw breakpoints, internal bus and ports
**Core only includes the core pipeline only
SiFive 7 Series RISC-V Core IP
SiFive Core IP
7 series:

The highest performance commercial RISC-V processor IP

Common Feature sets
Hard Real-time capabilities
Unprecedented scalability

32-bit Embedded Processors
64-bit Embedded Processors
64-bit Application Processors

~60% increase in CoreMarks/MHz*
~40% increase in DMIPS/MHz*
10% increase in Fmax*

*Compared to SiFive 5 series
U7 Series Features

Ultra High Performance 64-bit RISC-V Multi-Core Application Processor

- **Multi-Core Architecture**
  - Allows for instantiation of up to 9 U7 and/or S7 cores as well as a configurable Level 2 Cache

- **U7 Core Architectural Features**
  - RV64GCV capable core with Sv39 Virtual Memory Support
  - Dual Issue, in-order 8 stage Harvard Pipeline

- **Functional Safety and Security and Real Time features**
  - SECDED ECC on all L1 and L2 memories
  - User Mode Interrupts for compartmentalization
  - Programmatically clear and/or disable dynamic branch prediction for deterministic execution and enhanced security

- **Configurable EXX minion cores can provide a variety uses**
  - System boot and monitor, Sensor Hub/Fusion, Security Co-Processor

**Broad market applications**
- General purpose embedded, industrial, IoT, high-performance real-time embedded, automotive
U7 Series Standard Cores

- High performance 7 Series Processor
  - 0.577 in TSMC 28HPC for entire Core Complex including CLIC, Debug, and Several Ports
  - 2.5 DMIPS/MHz, 4.9 Coremarks/MHz

- Pre-Integrated Heterogeneous in-cluster CPU combinations
  - Up to 9 fully coherent Processors in a single core complex

- Deterministic, Low Latency, Interrupt Response
  - CLIC for fast, core specific, deterministic interrupt handling
  - PLIC on the U74-MC for multi-core interrupt distribution

<table>
<thead>
<tr>
<th>Core Complex Area (mm²)*</th>
<th>0.577</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Only Area (mm²)**</td>
<td>0.269</td>
</tr>
<tr>
<td>Core Complex Power – Dhrystone (mW) @ worst setup frequency (includes leakage)</td>
<td>106</td>
</tr>
<tr>
<td>Power Characterization Corner</td>
<td>func_tt_0p9v_25c_typical</td>
</tr>
</tbody>
</table>

Note: All area and power numbers do not include RAMs
*Core Complex includes the Core plus Level 2 Cache Controller, Interrupt Controller w/255 irq and 7 priority levels, Debug w/ 4 hw breakpoints, internal bus and ports
**Core only includes the core pipeline, and L1 memory interfaces
SiFive Custom Instruction Extension (SCIE)
SiFive Custom Instruction Extension (SCIE)

- The SCIE creates a **Verilog black box for your custom instruction**
  - The CII has a simple pre-defined interface and is the same across the entire SiFive product portfolio
  - Custom Instructions can be created in Verilog with an existing EDA flow

- The SCIE allows for operations on the Integer register file
  - \( rs1 \) and \( rs2 \) are decoded by the core and provided over the SCIE, no register copies necessary
  - \( rd \) is used to pass destination register data back to the core

- **Tightly coupled to the core**
  - Core pipeline handles all hazards

- **Flexible custom instruction support**
  - Support for 1 or 2 cycle instructions
SiFive Silicon and Development Platforms
HiFive1: Arduino-Compatible RISC-V Dev Board

- SiFive FE310-G000 (built in 180nm)
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: Both 3.3 V or 5 V supported
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 16 MB Quad SPI
- Host Interface (microUSB): Program, Debug, and Serial Communication
Freedom Everywhere 32-bit Low-power microcontroller platform

- 320+ MHz SiFive E31 CPU
  - 16KB L1I$, 16KB Data Scratchpad
  - Hardware Multiply/Divide, Debug Module
- Multiple Power Domains
- Low-Power Standby
- Wide Range of Clock Inputs

Freedom E310, QFN48, manufactured in TSMC 180nm
HiFive Unleashed: World’s First Multi-Core RISC-V Linux Dev Board

- SiFive FU540-C000 (built in 28nm)
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards
Freedom Unleashed 64-bit Multi-Core RISC-V Linux Platform

• 1.5+ GHz U54-MC SiFive CPU
  • 1x S51: 16KB L1I$, 8KB DTIM with ECC support
  • 4x U54: 32KB L1I$, 32KB L1D$ with ECC support
  • Single- and Double-precision floating-point support
  • 2MB Banked L2$ with directory-based cache-coherence & ECC support
• ChipLink
  • Serialized Chip-to-Chip Coherent TileLink Interconnect
• DDR3/4, GbE, Peripherals
お問い合わせ

SiFive社各プロダクトに関するお問い合わせ、および、サポートは以下の窓口にて承ります

ご連絡をお待ちしております

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サポート窓口：support-sifive@dts-insight.co.jp